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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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R C van Dijk

DEN HAAG, DEN
THE HAGUE,
LA HAYE, LE 10/05/04

Field of the Invention

This invention relates to the field of electronic system packaging. More particularly the invention relates to assembly incorporating at least three microelectronic chips on which integrated devices are formed, said chips being stacked together and at least one of the chips including via holes running through said chip and filled with conductive material. The invention also relates to a microelectronic chip intended to be used in such an assembly and to a packaged system including at least such an assembly. At last, the invention relates to a method to manufacture such an assembly.

Background of the Invention

Such assembly is known in document US 2001/0006257. In this document a method to realize an assembly of at least three microelectronic chips on which integrated devices are formed, said chips being stacked together and at least one of the chips including via holes running through said chip and filled with conductive material.

In this document chips are stacked one on the other by inserting an adhesive layer between each pair of chips. Holes are realized once the chips are superposed and through the top chip and filled with conductive material. This implies that said holes are realized in a dedicated part of the chip in order not to destroy the devices integrated on the chips. The assembly proposed in this document is an assembly of similar active chips. Once the three chips are superposed and connected, the connection to external circuits or to passive elements has to be realized through a protective layer coated on the highest chip.

The assembly proposed in this document of the prior art therefore presents drawbacks and limitation regarding the quality of the miniaturization and the implementation of such an assembly for complex systems.

Summary of the Invention

It is an object of the present invention to propose a miniaturized and an easy to implement assembly of several microelectronic chips, even for complex systems.

This is achieved with a microelectronic chip assembly as presented in the introductory paragraph and such that said chip including via holes, called intermediate chip, is realized from a high ohmic substrate on which are formed devices for the functioning of at least two other microelectronic chips, called top and bottom chips, connected by flip chip bonding respectively on top and bottom faces of said intermediate chip, said via holes being electrically connected to pads of said top and bottom chips.

This assembly enables to prepare the intermediate chip first and independently of the assembly steps. Consequently, via holes are realized during manufacture of said intermediate

chip among the integrated devices and no specific surface needs to be dedicated to them on said intermediate chip. A very good miniaturization is therefore obtained.

It is advantageous that said intermediate chip is manufactured independently from a high ohmic substrate on which specific devices are formed for the functioning of the two other microelectronic chips. Effectively, for example, if only passive devices are formed, masks are simple and intermediate chip is thus very cheap.

As top and bottom chips are connected by flip chip bonding, this assembly enables to avoid the use of wires that introduce parasitic elements, which limit performances and particularly the high frequency performances. Particularly the invention enables to have short and efficient connections with devices integrated on said intermediate chip and dedicated to the functioning of the top and bottom chips.

This assembly can be easily packaged by connecting said intermediate chip by flip chip bonding in order that said intermediate chip is linked to an external connection device enabling the connection with external circuits. Therefore, communications with external circuits are easy to implement and of good quality. Advantageously said connection device is a lead frame type of package or a substrate that is then packaged. In the case where several intermediate chips are present in the assembly, only one intermediate chip is linked to said connection device by flip chip bonding.

This invention can be used with chips on which are formed any kind of devices. Nevertheless, it occurs that the functioning of a whole system constituted by the assembly is not optimum due to interference between the different integrated devices that are very close to each other. For example, devices operating at high frequency are very sensitive to parasitic elements or high power devices can generate damages in very compact assembly as the one of the invention.

In an advantageous embodiment, devices integrated on said bottom, intermediate and top chip are chosen in order that said devices are stacked in a specific order relatively to said connection device enabling high performance for said assembly. This specific order is such that high performance sensitive devices are integrated on bottom chip while low performance sensitive devices are integrated on top chip.

This enables to have short connections for performance sensitive devices and to optimize the linking of the different device of the assembly. Effectively, high frequency signal path and high power signal path require very low ohmic, low inductive or low impedance routing in order to preserve the high frequency behaviour and to maximize the energy yield of the power devices respectively. The implementation of high frequency or high power devices is thus advantageously realized on the chip that is the closest to the connection device and consequently on bottom chips.

In a preferred embodiment, said connection device includes a heatsink dedicated to be in contact with said bottom chip.

This enables to have heat dissipative devices in contact with said heatsink. In such a case, heat dissipative devices are integrated on said bottom chip. Effectively, as the resulting assembly is very compact, strong heat dissipation can be generated within an assembly of the invention. Heat dissipation is generally the result of high frequency (non, high power is not always linked to high frequency) or high power devices integrated on the bottom chip.

In a specific embodiment, at least a heat dissipative device is integrated on said bottom chip, said bottom chip being in contact with said heat-sink.

In a specific embodiment, at least a high frequency device is integrated on said bottom chip, said bottom chip being in contact with said heat-sink.

The preferred embodiment enables to separate devices as temperature sensitive ones with heat dissipative devices and to make closer devices that are dedicated to work in high frequency.

In a specific implementation, devices are integrated on both sides of said intermediate chip. Such a characteristic enables to have more devices on said intermediate chip. For example, devices dedicated to the functioning of the top chip are integrated on the top side and devices dedicated to the functioning of the bottom chip are integrated on the bottom side. Via holes are used to realize connection between the both types of devices and for the direct connection of the top and the bottom chips.

The invention also relates to a packaged system including at least three devices that are integrated on separated chips that are arranged in an assembly according to the invention. An example of such a system is given in the following.

The invention relates at last to a method to manufacture a miniaturized packaged system including at least a microelectronic assembly. It comprises step of realizing at least one chip, called intermediate chip, including integrated devices on at least one face and via holes running through said chip and filled with conductive material, from a high ohmic substrate. Then, according to the method of the invention is realized a step of linking at least one chip, called bottom chip and including integrated devices on one face, by flip chip bonding on said intermediate chip, in order that said via holes are in connection with terminal pads of said bottom chip. The intermediate chip is then linked by flip chip bonding on a connection device in order that said bottom chip is stacked between said intermediate chip and said connection device. Then is realized a step of linking by flip chip bonding a third chip, called top chip and including integrated devices on one face, on said intermediate chip, in order that said via holes are in connection with terminal pads of said top chip. At last the assembly is moulded in a moulding component.

Such a method enables to obtain a very compact system presenting the same functionalities than a larger one if realized by other techniques like integration on a single chip. Therefore, such a method avoids an integration of devices of different kinds on a same chip. The different chips are effectively realized independently and then assemble according to the invention.

Brief Description of the Drawings

The invention is described hereafter in detail in reference to the diagrammatic figures wherein:

Fig. 1 represents a microelectronic chip assembly according to the invention;

Fig. 2 illustrates an example of application for a system of the invention;

Fig. 3 illustrates the steps of a method to manufacture a miniaturized packaged system according to the invention.

Description of embodiments

The terms 'top' and 'bottom' are used herein to indicate directions relative to the structure of the microelectronic chip assembly itself or to a connection device. It should be understood that these terms are used to refer to the frame of reference of the assembly itself or to said connection device, and not to the ordinary, gravitational frame of reference.

The term 'device' designates any component, function, circuit, application that can be integrated on a microelectronic chip.

Figure 1 represents a microelectronic chip assembly ASY according to the invention. This assembly includes three microelectronic chips TCH, ICH, BCH on which integrated devices are formed. Integrated devices are integrated using semi-conductor or semi-insulating technologies.

Terminal pads PAD are symbolized by a larger line on this figure. These terminal pads are made of conductive material coated on chip. Said terminal pads are part of the integrated devices formed on chips.

The three chips are stacked together. One of the chips called intermediate chip ICH includes via holes VH running through said intermediate chip ICH and filled with conductive material. Said via holes are linked to terminal pads integrated on at least one surface of said intermediate chip ICH. Said intermediate chip ICH thus can also include terminal pads on both sides: bottom face BF and top face TF.

The two other microelectronic chips, called top and bottom chips TCH and BCH, are connected by flip chip bonding on top face TF and bottom face BF of said intermediate chip ICH. Said top and bottom chips TCH and BCH are thus linked to said intermediate chip ICH by an electrical connection as known in the flip chip bonding field.

The flip chip bonding interconnection method offer a short signal path and consequently a more rapid communication between devices that can other methods, such as tape automated bonding or conventional wire bonding. Moreover, bonded terminal pads are not restricted to the periphery of the chip. Terminal pads are located at points of interconnection. For example, bumps are formed by plating of several layers of metals on the terminal pads of the chip

dedicated to be connected by flip chip bonding. Following deposition, the chip is heated to reflow the metals, thus causing surface tension of the deposit to form hemispherical solder bumps. Therefore top and bottom chips are subsequently severed from the wafer of which it was a part and flipped for alignment with the terminal pads and/or the via holes VH on said intermediate chip ICH. These bumps are thus contacted with the terminal pads and/or via holes VH of said intermediate chip ICH and uniformly heated to simultaneously form interconnection between terminal pads of intermediate chip aligned with the ones of top and bottom chips. A method describing the different steps using such flip chip bonding is presented hereinafter. Any other technique to realize a flip chip bonding between two chips can also be used. For example, an adhesive layer including micro balls of conductive material to realize electrical connections can also be used in order to realize the bonding and the connection without any bumps. Such techniques and others are well known within microelectronic field.

The main advantage of flip chip bonding is that connections are direct and avoid the use of wires. According to the invention, said via holes VH are directly connected to pads of said top and bottom chips in order to realize electrical connections directly between top and bottom chips or between intermediate chip and top or bottom chip.

The assembly constituted by the three chips is then disposed on a connection device CDV that can be a substrate or a lead frame. Connection between said substrate or lead frame and the assembly is realized by linking said intermediate chip ICH by flip chip bonding with said connection device CDV. This connection device CDV enables the connection with external circuits. Such a connection device CDV is well known by the man skilled in the art of packaging.

In a preferred embodiment, the connection device includes a heat sink that is intended to be in contact with the bottom chip BCH. This enables the evacuation of energy that could accumulate in the assembly of the invention. As the invention enables to have a very compact system, this feature is important as energy could accumulate and deteriorate the system.

According to the invention, the different devices integrated on different chips are interconnected to each other by using intermediate chip, which contains the necessary peripheral devices to make the different devices integrated on top and bottom chips working.

Figure 2 represents an example of application for a system of the invention. It consists in an electronic function for which the necessary devices can be splitted across three chips. In such a case the invention permits to optimize the performance and cost.

The invention is thus very advantageous when different kind of devices requiring different manufacturing requirements need to be present in a system. For example, a system is constituted of power device, of passive devices possibly having to be in connection with said power devices. Signal processing devices are also generally part of the system. All these different devices require different kinds of integration. The invention enables to build a system comprising

all these devices in a compact way while keeping a very simple manufacturing process. Effectively, the different chips comprising the different kind of devices are formed separately before being connected to each other by the method of the invention.

On figure 2, an illustrative example is proposed. This illustrative example includes an integrated high frequency transceiver TSC and a digital base-band solution BB. Said high frequency transceiver TSC requires passive devices MD comprizing at least inductors and decoupling capacitors as well as high frequency matching devices. The invention enables to divide these different devices among three different chips. Said high power and high frequency devices are advantageously integrated on the bottom chip in order to be close to the heat-sink in the preferred embodiment of the invention. Therefore, the passive devices MD can be integrated on the intermediate chip ICH in order to have short connections to high power and high frequency devices formed on bottom chip. This implementation enables also good connection to ground for high frequency devices through said intermediate chip ICH connected to said connection device. Effectively RF front-end section of the transceiver requires high quality ground connection. The invention has an economical advantage as matching devices like inductors are build on the intermediate chip realized on cheap high ohmic substrate. Moreover the integration of passive devices requires the use of less masks than, for example, the integration of digital devices. It renders cheap the resulting intermediate chip. The digital base-band and programmable circuitry is realized on the top chip TCH. Effectively such devices work correctly even under low quality ground connection. Moreover, they are generally not heat dissipative.

Consequently a specific order from the bottom to the top chip is here presented.

In this example, the intermediate chip is integrated on a single face wherein are formed the passive elements for the high frequency and power devices formed on bottom chip. Contacts with top chip are provided by said via holes formed through intermediate chip. The invention includes also the case where devices are formed on both sides of said intermediate chip. In this case, devices that are dedicated to interact with devices formed on top chip are integrated on the second side of said intermediate chip.

Therefore according to the invention, one full package system includes digital low power devices, high power devices, memories, analog devices, high frequency small signal devices, high power analog devices, high frequency devices. This last list is not exhaustive. By generalization of the invention to any kinds of devices present in the system, the specific order of the advantageous embodiment is, from the bottom to the top, from performance sensitive devices like high frequency device to low performance sensitive device like digital devices having low power consumption.

According to this specific order, power devices including digital devices with high power consumption are formed on a bottom chip directly in contact with the heat-sink. High frequency devices including radio frequency devices are also directly in contact with the heat-sink. High

performance analog devices are also formed on a bottom chip. This enables good power dissipation and low impedance ground connection necessary for high frequency devices. The different kind of devices can be integrated on one single bottom chip or on several bottom chips. Thus any performance sensitive devices are advantageously implemented on said bottom chips.

According to this specific order, applications of the devices formed on bottom chip are advantageously integrated on the bottom face BF of said intermediate chip ICH. Such applications include matching devices in the above presented example. If ever said applications are integrated on the top face TF, interconnection with devices integrated on said bottom chip are realized by via holes through intermediate chip. Nevertheless connections of said bottom chip is of less good quality than if said applications are implemented on the bottom face. Effectively connections are longer as they comprise the via holes connection.

According to the specific order, the top chip or several top chips include low power devices, low frequency analog devices, low power digital devices and memories. This last list is not exhaustive, any low performance sensitive devices are advantageously integrated on said top chips. Said top chips are linked to said intermediate chip by flip chip bonding and connections with devices integrated on intermediate and bottom chips are provided by via holes.

The top face TF of the intermediate chip advantageously comprises the necessary devices to make devices integrated on top chip working properly. It can also be noted that ground connections are still of good quality as top chips are directly connected to intermediate chip that is connected to ground through the connection device.

Thus the invention proposes an optimized multi-application assembly. The invention enables to achieve an optimized system performance. In extension of the invention several sandwiches of chips can be stacked in order to cope with multiple applications. In such an extension, several intermediate chips are needed. Nevertheless the order, from the bottom to the top needs to be kept from high power consumption, high frequency applications, devices requiring low impedance connections to low power, low frequency applications. For example, the specific order is from high power to low power devices and from high frequency to low frequency devices from the bottom to the top. A general characterization of the specific order is from high performance sensitive devices to low performance sensitive devices.

Figure 3a to 3f describes the main steps of a method of the invention to manufacture a miniaturized packaged system including at least a microelectronic assembly according to the invention.

Figure 3a represents a wafer WAF on which are formed the intermediate chips ICH. On the figure 3a is only represented one intermediate chip ICH. Others are integrated beside it on said wafer represented by dotted line. Said intermediate chip includes integrated devices on at least

one face and via holes VH running through said chip and filled with conductive material. Said via holes VH are realized according to well known microelectronic technique.

Bottom chips are realized separately. They include integrated devices on one face. Then at least one bottom chip is linked by flip chip bonding to said first wafer in order that terminal pads of said bottom chip is aligned with terminal pads, notably the ones in connection with said via holes of said intermediate chip. This is represented on figure 3b. Bottom chips are linked to the bottom face BF of said intermediate chip ICH. The 'bottom' representation on figure 3 is relative to the final assembly and not to the different position that can be taken by intermediate chip and other chips during the method.

Then said wafer on which are flipped said bottom chips is cut. A microelectronic intermediate assembly as represented on figure 3c is thus obtained.

Said intermediate chip with flipped bottom chip is then linked by flip chip bonding to a connection device CDV. Said bottom chip is thus stacked between said intermediate chip and said connection device CDV. Advantageously, said bottom chips are put in contact with a heat-sink as presented above. Said heat-sink is part of said connection device. Thus said bottom chip is stacked between said intermediate chip and said heat-sink as represented on figure 3d.

A third chip called top chip is then linked by flip chip bonding to the top face TF of said intermediate chip by aligning said via holes with pads on said top chip. Figure 3e represents the resulting assembly.

At last, according to packaging technology, the assembly is moulded in a moulding component MC. A packaged system as represented on figure 3f is thus obtained.

Presented figures are illustrative of special embodiments of the invention and are not restrictive. It will be apparent to those skilled in the art that many modifications and variations may be made to the exemplar embodiments of the present invention list forth above, without departing substantially from the principles of the present invention. All such modifications and variations are intended to be included herein.

Claims:

1. A microelectronic chip assembly comprising at least three microelectronic chips stacked together and on which integrated devices are formed, at least one of the chip including via holes running through said chip and filled with conductive material, characterized in that said chip including via holes, called intermediate chip, is realized from a high ohmic substrate on which are formed devices for the functioning of at least two other microelectronic chips, called top and bottom chips, connected by flip chip bonding respectively on top and bottom faces of said intermediate chip, said via holes being electrically connected to pads of said top and bottom chips.

2. An assembly as claimed in Claim 1, wherein said intermediate chip being also linked by flip chip bonding in order to be connected to an external connection device enabling the connection with external circuits.

3. An assembly as claimed in Claim 2, wherein devices integrated on said bottom, intermediate and top chip are chosen in order that said devices are stacked in a specific order relatively to said connection device enabling high performance for said assembly, said specific order being such that high performance sensitive devices are integrated on bottom chip while low performance sensitive devices are integrated on top chip.

4. An assembly as claimed in one of the Claims 2 and 3, wherein said connection device includes a heatsink dedicated to be in contact with said bottom chip.

5. An assembly as claimed in Claim 4, wherein at least a heat dissipative device is integrated on said bottom chip, said bottom chip being in contact with said heat-sink.

6. An assembly as claimed in Claim 4, wherein at least a high frequency device is integrated on said bottom chip, said bottom chip being in contact with said heat-sink.

7. An assembly as claimed in one of the Claims 1 and 2, wherein said intermediate chip includes integrated devices on both sides.

8. A packaged system including at least three devices that are integrated on separated chips, characterized in that said chips are arranged in an assembly as claimed in one of the claims 1 to 7.

9. A method to manufacture a miniaturized packaged system including at least a microelectronic assembly, characterized in that said method includes the steps of:
   - Realizing at least one chip, called intermediate chip, including integrated devices on at least one face and via holes running through said chip and filled with conductive material, from a high ohmic substrate,
   - Linking at least one chip, called bottom chip and including integrated devices on one face, by flip chip bonding on said intermediate chip, in order that said via holes are in connection with terminal pads of said bottom chip,
   - Linking the intermediate chip by flip chip bonding on a connection device in order that said bottom chip is stacked between said intermediate chip and said connection device,
   - Linking by flip chip bonding a third chip, called top chip and including integrated devices on one face, on said intermediate chip, in order that said via holes are in connection with terminal pads of said top chip,
   - Moulding the assembly in a moulding component.

"Optimized multi-application assembly".

Abstract:

The invention relates to a microelectronic chip assembly ASS comprising at least three microelectronic chip ICH, TCH, BCH stacked together and on which integrated devices are formed. At least one of the chip, called intermediate chip ICH, includes via holes VH running through said chip ICH and filled with conductive material is realized from a high ohmic substrate on which are formed devices for the functioning of at least two other microelectronic chips, called top chip TCH and bottom chip BCH. Said top and bottom chips TCH and BCH are connected by flip chip bonding respectively on top face TF and bottom face BF of said intermediate chip Ich and said via holes VH are electrically connected to pads of said top and bottom chips TCH and BCH.

FIG. 1

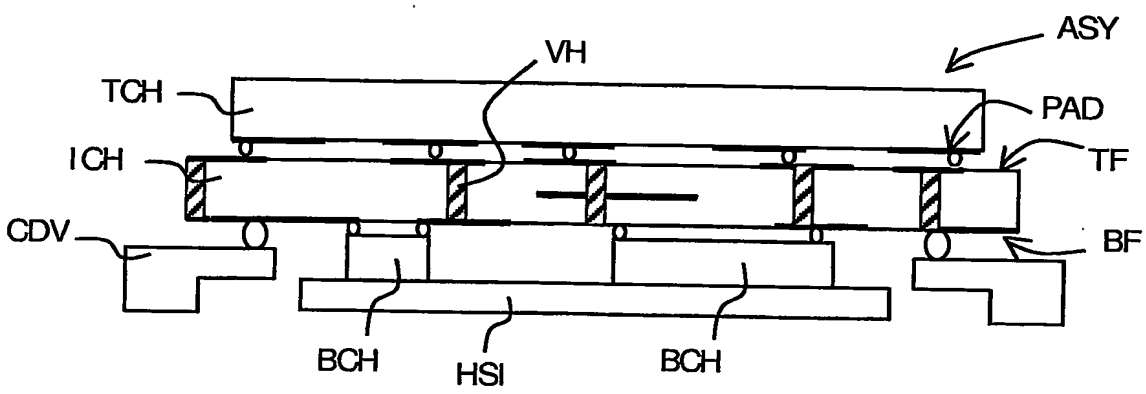

FIG.1

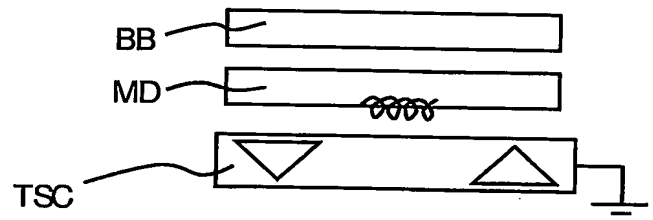

FIG.2

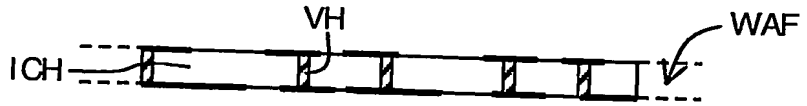

FIG.3a

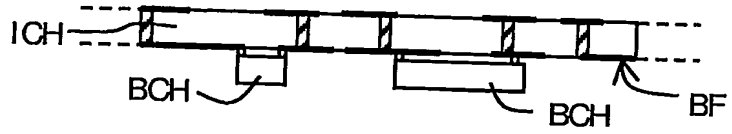

FIG.3b

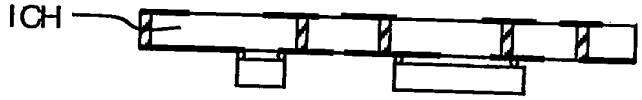

FIG.3c

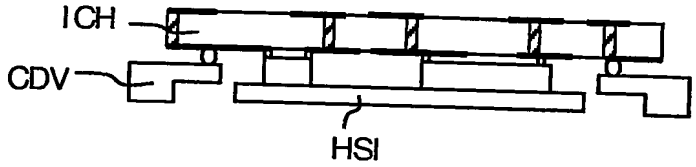

FIG.3d

FIG.3e

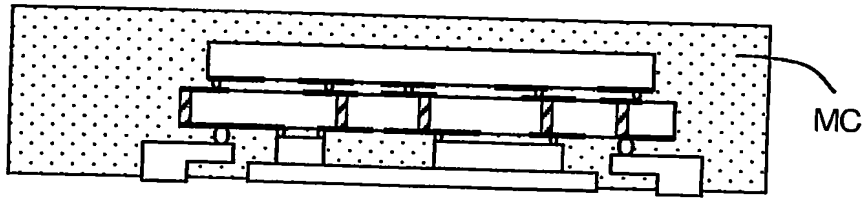

FIG.3f